

REMARKS

Upon entry of the present amendment, claims 1-19 will have been canceled and new claims 20-35 will have been submitted for entry by the Examiner. In view of the herein contained amendments and remarks, Applicants respectfully request reconsideration and withdrawal of the outstanding rejections and an indication to such effect in due course.

Applicants note with appreciation the Examiner's consideration of the documents cited in the Information Disclosure Statement filed in the present application by the return of the initialed and signed copy of the PTO-1449 Form accompanying the Information Disclosure Statement filed herein.

Applicants further note with appreciation the Examiner's acknowledgment of Applicants claim for foreign priority under 35 U.S.C. § 119 and the filing of the certified copies of the priority documents.

Applicants finally note with appreciation the Examiner's indication that claims 3, 6, 7, and 10 would be allowable if rewritten in independent form.

In the outstanding Official Action, the Examiner rejected claims 9, 11, 13, 15, 16, 18 and 19 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Because claims 9, 11, 13, 15, 16, 18 and 19 have been canceled, Applicants respectfully assert that the 35 U.S.C. § 112, second paragraph, rejection is moot.

In the outstanding Official Action, the Examiner rejected claims 1, 2, 4, 5, 8, 14 and 17 under 35 U.S.C. § 102(e) as being anticipated by YAMADA. Further, claims 9, 15 and 18 are rejected under 35 U.S.C. § 102(b) as being anticipated by W. CHEN et al. Finally, claims 11-13, 16 and 19 are rejected under 35 U.S.C. § 102(e) as being anticipated by X. CHEN et al.

One feature of the present invention, as generally recited in the combination of new independent claims 20 and 33 is to, inter alia, shift the phase of sampling timings at a time interval longer than a symbol duration, estimate the first synchronization timing and the second synchronization timing that correspond to the above sampling timings, respectively, and then from these synchronization timings, estimate a third synchronization timing. In other words, the above first feature is to estimate synchronization timings at multiple sampling timings of different phases at every time interval, the interval being longer than a symbol duration, and, using the estimated synchronization timings, to estimate a definitive synchronization timing.

This feature of the present invention at least has the advantage of enabling synchronization timing estimation with a higher degree of time resolution without substantially increasing the sampling rate of received signals. As a result, it is possible to reduce power consumption and cost.

Another feature of the present invention, as generally recited in the combination of new independent claims 28 and 34 is, inter alia, a table that has operation value ratios stored therein in association with plural short times. A first synchronization timing is determined based on a result of a correlation operation using a known signal sequence and a second synchronization timing, that is more accurate than the first synchronization timing, and that is estimated with reference to the table as disclosed in the specification, for example, on page 6, lines 18-23.

Yet another feature of the present invention, as generally recited in the combination of new independent claims 31 and 35 is, inter alia, to cancel inter symbol interference using multiple tap coefficients stored in association with short times. An estimate is determined based on a synchronization timing from the short time corresponding to the tap coefficient that maximizes the correlation operation result between a signal after interference cancellation and a known signal sequence.

The above features of the present disclosed invention have at least the advantage of enabling synchronization timing estimation at a higher degree of time resolution, without substantially increasing the sampling rate for received signals as noted at page 52, lines 9-19 of the specification. As a result, it is possible to reduce power consumption and cost.

In contrast to the above-noted features of the present invention, YAMADA (U.S. Patent No. 6,501,811) discloses a receiving apparatus having sampling means which

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performs sampling of a received signal at the instant $-T/4$, which is shifted from the reference sampling time point T , and a sampling at the instant $+T/4$, having a phase difference from the first sampling. In other words, YAMADA discloses a sampling system that shifts the phase so as to perform sampling at double sampling rates.

However, YAMADA fails to disclose the synchronization timing estimation of the present disclosed invention. That is, YAMADA merely discloses a sampling system, in which, as recited in YAMADA's claim 1, includes a second sampler that alternately outputs two low pass filter outputs having respective phases at a sampling period that is half a fixed sampling period T . In other words, the phase of a sampling timing is shifted at a time interval half the fixed sampling period T , double the sampling rate as compared to the normal rate. Particularly, YAMADA's sampling period refers to a normal signal sampling timing, which means that sampling needs to be performed at least once for every symbol and that the phase of the sampling timing is shifted at every time interval shorter than a symbol duration.

In contrast to YAMADA, in the present disclosed invention, the phase of a sampling timing is shifted at a time interval longer than a symbol duration. Additionally, as described in the specification, this time interval is sufficiently long in comparison to the symbol duration (e.g., several bursts). As a result, in the present disclosed invention it is possible to increase the time resolution of a synchronization time estimation without increasing the sampling rate.

Thus, YAMADA contains no disclosure or suggestion of the above-noted feature of the invention, to estimate synchronization timings at multiple sampling timings of different phases at every time interval. The phase interval is longer than a symbol duration and using the estimated synchronization timings to estimate the definitive synchronization timing.

Moreover, U.S. Patent No. 5,796,787 to W. CHEN discloses a reception apparatus estimating the timing of a received signal at a predetermined sampling rate and another timing estimation means for performing a correlation of the previous timing estimate and a known signal. However, W. CHEN contains no disclosure or suggestion of the above-noted feature of a table that has operation value ratios stored therein in association with a plurality of short times. Moreover, a first synchronization timing is determined based on a result of a correlation operation using a known signal sequence. A second synchronization timing, that is more accurate than the first synchronization timing, is estimated with reference to the table. In particular, there is no disclosure or suggestion in W. CHEN of an operation value ratio table that has ratios between multiple correlations stored therein as disclosed in the present invention.

Further, U.S. Patent No. 6,366,629 to X. CHEN discloses a reception apparatus having means for storing tap coefficients for removing inter-symbol interference, a filter for filtering the received signal, and timing estimating means for performing a timing estimation based on the filtering results. However, X. CHEN contains no disclosure or suggestion of

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the above-noted feature of canceling inter symbol interference using multiple tap coefficients stored in association with short times, and estimating a synchronization timing from the short time corresponding to the tap coefficient that maximizes the correlation operation result between a signal after interference cancellation and a known signal sequence.

In view of the herein contained claims and remarks, Applicants respectfully submit that none of the subject matter recited in the new independent claims is anticipated by YAMADA, W. CHEN and X. CHEN, and respectfully submit that the outstanding claim rejections under 35 U.S.C. § 102(e) and 35 U.S.C. § 102(b) have been overcome and that the present application is presently in condition for allowance.

Moreover, there is no suggestion or disclosure in YAMADA, W. CHEN, X. CHEN, or the prior art of record, that separately or in any proper combination render obvious the features of the present claimed invention.

Applicants have made a sincere effort to place the present application in condition for allowance and believe that they have now done so. Applicants have pointed out the specific language of Applicants' claims that define over the references of record and respectfully request an indication to such effect, in due course.

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Should the Examiner have any questions or comments regarding this Response, or the present application, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully submitted,
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